AMENDMENTS TO THE CLAIMS

The following is a complete listing of revised claims with a status identifier in parenthesis.

LISTING OF CLAIMS

1. (Currently Amended) A display device which selects each line of a screen having pixels aligned in a matrix manner and provided in a display section by applying a scanning signal to a scanning signal line of a pixel of each line so as to scan the screen, and supplies a data signal from a data signal line to a pixel of a selected line so as to carry out display, comprising:

a driving control circuit which (a) generates, as a driving control signal, a control clock signal based on at least a base clock signal, the control clock signal defining an inaction period where all scanning signal lines become non-scanning state, the inaction period being provided between scanning periods for scanning the screen, and which (b) stops driving of driving circuits provided for driving the display section, the driving control circuit stopping driving of the driving circuits in the inaction period; and

a clock signal generation circuit for generating a clock signal which is used for taking the data signal into the data signal line, the clock signal being faster than the control clock signal and the base clock signal; wherein

the driving control circuit stops driving of the clock signal generation circuit in the inaction period, in addition to stopping driving of the driving circuits, and maintains driving for obtaining at least one of the clock signals other than the clock signal, and

the base clock signal, the clock signal and the control clock signal have different speeds.

2. (Currently Amended) A display device which selects each line of a screen having pixels aligned in a matrix manner and provided in a display section by applying a scanning signal to a scanning signal line of a pixel of each line so as to scan the screen, and supplies a data signal from a data signal line to a pixel of a selected line so as to carry out display, comprising:

a driving control circuit which (a) generates, as a driving control signal, a control clock signal that defines an inaction period where all scanning signal lines become non-scanning state, the inaction period being provided between scanning periods for scanning the screen, and which (b) stops driving of driving circuits provided for driving the display section, the driving control circuit stopping driving of the driving circuits in the inaction period;

a clock signal generation circuit for generating a clock signal which is used for taking the data signal into the data signal line, the clock signal being faster than the control clock signal;

the driving control circuit stopping driving of the clock signal generation circuit in the inaction period, in addition to stopping driving of the driving circuits and maintaining driving for obtaining at least one of the clock signals other than the clock signal,;

an output timing clock generation circuit for generating an output timing clock which is used as an output timing signal of a driving signal to the display section from the driving circuits,

wherein:

the clock signal generation circuit generates the clock signal based on the output timing clock generated by the output timing clock generation circuit, and the driving control circuit stops driving of the output timing clock generation circuit in the inaction period, and

the output timing clock, the control clock signal and the clock signal have different speeds.

3. (Currently Amended) A display device which selects each line of a screen having pixels aligned in a matrix manner and provided in a display section by applying a scanning signal to a scanning signal line of a pixel of each line so as to scan the screen, and supplies a data signal from a data signal line to a pixel of a selected line so as to carry out display, comprising:

a driving control circuit which (a) generates, as a driving control signal, a control clock signal that defines an inaction period where all scanning signal lines become non-scanning state, the inaction period being provided between scanning periods for scanning the screen, and which (b) stops driving of driving circuits provided for driving the display section, the driving control circuit stopping driving of the driving circuits in the inaction period;

a clock signal generation circuit for generating a clock signal which is used for taking the data signal into the data signal line, the clock signal being faster than the control clock signal;

the driving control circuit stopping driving of the clock signal generation circuit in the inaction period, in addition to stopping driving of the driving circuits, and maintaining driving for obtaining at least one of the clock signals other than the clock signal;

an output timing clock generation circuit for generating an output timing clock which is used as an output timing signal of a driving signal to the display section from the driving circuits; and

a start timing clock generation circuit for generating a start timing clock which is used as a scanning start timing signal of the driving circuits,

wherein:

the output timing clock generation circuit generates the output timing clock based on the start timing clock generated in the start timing clock generation circuit, the clock signal generation circuit generates the clock signal based on the output timing clock generated by the output timing clock generation circuit and the driving control circuit stops driving of the start timing clock generation circuit in the inaction period, based on the control clock signal, and

the start timing clock, the control clock signal and the clock signal have different speeds.

4. (Currently Amended) A display device which selects each line of a screen having pixels aligned in a matrix manner and provided in a display section by applying a scanning signal to a scanning signal line of a pixel of each line so as to scan the screen, and supplies a data signal from a data signal line to a pixel of a selected line so as to carry out display, comprising:

a driving control circuit which (a) generates, as a driving control signal, a control clock signal based on a base clock signal, the control clock signal defining an inaction period where all scanning signal lines become non-scanning state, the inaction period being provided between scanning periods for scanning the screen, and which (b) stops driving of driving circuits provided for driving the display section, the driving control circuit stopping driving of the driving circuits in the inaction period;

a clock signal generation circuit for generating a clock signal, the clock signal being used for taking the data signal into the data signal line, the clock signal being faster than the control clock signal;

the driving control circuit stopping driving of the clock signal generation circuit in the inaction period, in addition to stopping driving of the driving circuits, and maintaining driving for obtaining at least one of the clock signals other than the clock signal; wherein

the clock signal generation circuit is a clock signal oscillation circuit for oscillating a clock signal, and

the control clock signal, the clock signal and the base clock signal have different speeds.

5. (Original) The display device as set forth in claim 1, wherein:

liquid crystal display elements are used as the pixels.

6. (Currently Amended) A driving method for a display device which selects each line of a screen having pixels aligned in a matrix manner by applying a scanning signal to a scanning signal line of a pixel of each line so as to scan the screen, and supplies a data signal from a data signal line to a pixel of a selected line so as to carry out display, the driving method comprising:

generating, as a driving control signal, a control clock signal based on at least a base clock signal, the control clock signal defining an inaction period where all scanning signal lines become non-scanning state, the inaction period being provided between scanning periods for scanning the screen;

stopping driving of a clock signal generation circuit in the inaction period; while maintaining driving for obtaining at least one of the clock signals other than the clock signal, the clock signal generation circuit being for

generating a clock signal which is used for taking the data signal into the data signal line, the clock signal being faster than the control clock signal and the base clock signal; wherein

the base clock signal, the control clock signal and the clock signal have different speeds.

7. (Currently Amended) A display device which selects each line of a screen having pixels aligned in a matrix manner and provided in a display section by applying a scanning signal to a scanning signal line of a pixel of each line so as to scan the screen, and supplies a data signal from a data signal line to a pixel of a selected line so as to carry out display, comprising:

a driving control circuit which (a) generates, as a driving control signal, a control clock signal that defines an inaction period where all scanning signal lines become non-scanning state, the inaction period being provided between scanning periods for scanning the screen, and which (b) stops driving of driving circuits provided for driving the display section, the driving control circuit stopping driving of the driving circuits in the inaction period;

a clock signal generation circuit for generating a clock signal which is used for taking the data signal into the data signal line, the clock signal being faster than the control clock signal;

the driving control circuit stopping driving of the clock signal generation circuit in the inaction period, in addition to stopping driving of the driving circuits, and maintaining driving for obtaining at least one of the clock signals other than the clock signal; and

an output timing clock generation circuit for generating an output timing clock which is used as an output timing signal of a driving signal to the display section from the driving circuits,

wherein:

the clock signal generation circuit generates the clock signal based on the output timing clock generated by the output timing clock generation circuit, and

the control clock signal, the clock signal and the output timing clock have different speeds.

8. (Previously Presented) The display device as set forth in claim 7, further comprising:

a start timing clock generation circuit for generating a start timing clock which is used as a scanning start timing signal of the driving circuits,

wherein:

the start timing clock generation circuit generates the start timing clock based on the output timing clock generated in the output timing clock generation circuit.

9. (Previously Presented) The display device as set forth in claim 8, wherein:

the driving control circuit generates the control clock signal based on the start timing clock generated by the start timing clock generation circuit.

10. (Previously Presented) The display device as set forth in claim 2, further comprising:

a start timing clock generation circuit for generating a start timing clock which is used as a scanning start timing signal of the driving circuits,

wherein:

the output timing clock generation circuit generates the output timing clock based on the start timing clock generated in the start timing clock generation circuit.

11. (Previously Presented) The display device as set forth in claim 10, wherein:

the driving control circuit generates the control clock signal based on the start timing clock generated by the start timing clock generation circuit.

12. (Previously Presented) The display device as set forth in claim 1, wherein:

the clock signal generation circuit generates the clock signal based on the control clock signal generated by the driving control circuit.

13. (Previously Presented) The display device as set forth in claim 12, further comprising:

a start timing clock generation circuit for generating a start timing clock which is used as a scanning start timing signal of the driving circuits,

wherein:

the start timing clock generation circuit generates the start timing clock from the control clock signal generated by the driving control circuit.

14. (Previously Presented) The display device as set forth in claim 13, further comprising:

an output timing clock generation circuit for generating an output timing clock which is used as an output timing signal of a driving signal to the display section from the driving circuits,

wherein:

the clock signal generation circuit generates the clock signal from the output timing clock generated by the output timing clock generation circuit.

15. (Previously Presented) The display device as set forth in claim 14, further comprising:

an output timing clock generation circuit for generating an output timing clock which is used as an output timing signal of a driving signal to the display section from the driving circuits; and

a start timing clock generation circuit for generating a start timing clock which is used as a scanning start timing signal of the driving circuits,

wherein:

the start timing clock generation circuit generates the start timing clock from the output timing clock generated in the output timing clock generation circuit.

16. (Previously Presented) The display device as set forth in claim 15, wherein:

the driving control circuit generates the control clock signal based on the start timing clock generated by the start timing clock generation circuit.

17. (New) The display device of claim 1, wherein the clock signal has a fastest clock speed.

18. (New) The display device of claim 2, wherein the clock signal has a fastest clock speed.

19. (New) The display device of claim 3, wherein the clock signal has a fastest clock speed.

20. (New) The display device of claim 4, wherein the clock signal has a fastest clock speed.

21. (New) The method of claim 6, wherein the clock signal has a fastest clock speed.

22. (New) The display device of claim 7, wherein the clock signal has a fastest clock speed.